

What is claimed is:

1. A satellite modem, comprising  
a housing;  
a antenna for receiving and transmitting radio frequency (RF) signals;  
5 an upconverter/downconverter coupled to said antenna and adapted to upconvert RF  
signals from a first frequency band to a second frequency band, and adapted to  
downconvert RF signals from said second frequency band to said first  
frequency band;  
an RF transceiver coupled to said upconverter/downconverter and adapted to receive  
10 an output transmit signal and to generate an output RF signal therefrom, said  
RF transceiver adapted to receive an input RF signal from said  
upconverter/downconverter and generate an input receive signal therefrom;  
an intermediate frequency (IF) module adapted to receive said input receive signal  
and generate I and Q signals in response thereto;  
15 a baseband module adapted to receive said I and Q signals and to generate receive  
data in accordance therewith; and  
a baseband module adapted to generate said output transmit signal in accordance with  
a transmit data signal input thereto.
2. A receiver baseband apparatus, comprising:  
20 input means adapted to receive an I and Q signal;  
a first matched filter adapted to receive said I signal and generate an I filtered output  
therefrom;  
a second matched filter adapted to receive said Q signal and generate a Q filtered  
output therefrom;  
25 a processor programmed to perform the steps of:  
detecting the presence of signal activity as input to said receiver baseband  
apparatus;  
acquiring said signal once it is detected;  
pre-tracking said signal once it is detected;  
30 tracking said signal once it is detected;  
a decoder adapted to receive said I output signal and said Q output signal from said  
processor and to generate a decoded output therefrom;

09584746-00100  
SUBA77

a deinterleaver adapted to generate a deinterleaved output in accordance with said  
decoded output signal input thereto;  
a forward error correction decoder adapted to generate output receive data in  
accordance with said deinterleaved output signal input thereto; and  
5 a controller adapted to manage and control said input means, first matched filter,  
second matched filter, said processor, said decoder, said deinterleaver and said  
forward error correction decoder.

3. The apparatus according to claim 2, wherein said step of detecting the presence of  
signal activity comprises the steps of:

10 performing initial automatic gain control (AGC) on said signal;  
performing signal decimation; and  
performing signal detection and frequency acquisition.

4. The apparatus according to claim 2, wherein said step of acquiring said signal  
comprises the steps of:

15 inputting said signal to a first matched filter;  
performing a first automatic gain control (AGC) acquisition;  
performing timing acquisition;  
inputting said signal to a second matched filter;  
performing a second automatic gain control (AGC) acquisition;  
20 performing fine frequency estimation; and  
performing phase acquisition.

5. The apparatus according to claim 2, wherein said step of acquiring said signal  
comprises the step of performing coarse phase acquisition on said signal, wherein said step of  
performing coarse phase acquisition comprises the steps of:

25 rotating vectors  $z_n$  representing said signal into a single quadrant by an angle  $\Theta_k$ ;  
wiping off said  $z_n(\Theta_k)$  modulation;  
summing the wiped off vectors  $z_n(\Theta_k)$ ;  
determining the energy contained within a plurality of hypotheses; and  
selecting a single hypothesis from said plurality of hypotheses having the maximum  
30 energy.

6. The apparatus according to claim 2, wherein said step of pre-tracking comprises the steps of:

- inputting said signal to a matched filter;
- performing automatic gain control (AGC) tracking;
- performing timing tracking;
- performing phase tracking;
- generating I and Q soft decisions; and
- determining whether signal lock has been achieved.

7. The apparatus according to claim 2, wherein said step of pre-tracking comprises the steps of performing timing acquisition on K groups, each made up of N DFT estimates, each estimate calculated from blocks of 16 symbols, said step of performing timing acquisition comprising the steps of:

calculating a timing estimate  $t_i$  based on a DFT for 16 contiguous symbols,  $i = 1, \dots, N$ ,  
thereby obtaining  $N$  DFT estimates each based on a block of symbols;  
generating a histogram of said  $N$  DFT estimates  $t_i$ ;  
classifying a timing range said group the  $N$  estimates are in based on said histogram;  
unwrapping said  $N$  DFT estimates and calculating their average  $T_i$ ; and  
unwrapping  $K$  average estimates  $T_i$  and performing a least square fit of said  $K$   
averages so as to generate a final estimate.

8. The apparatus according to claim 1, wherein said decoder comprises a Viterbi decoder.

9. The apparatus according to claim 1, wherein said upconverter/downconverter is adapted to upconvert an L band signal to a C or Ku band signal.

10. The apparatus according to claim 1, wherein said upconverter/downconverter is adapted to downconvert a C or Ku band signal to an L band signal.

11. A receiver baseband apparatus, comprising:  
input means adapted to receive an I and Q signal;  
an I matched filter adapted to receive said I signal and generate an I filtered output therefrom;  
a Q matched filter adapted to receive said Q signal and generate a Q filtered output therefrom;

00534746-000100  
a processor programmed to:

perform automatic gain control (AGC) and generate an AG control signal therefrom;

perform timing detection and generate an A/D clock control signal therefrom;

perform phase detection and generate a voltage controlled oscillator (VCO) control signal therefrom;

a decoder adapted to receive said I output signal and said Q output signal from said processor and to generate a decoded output therefrom;

a deinterleaver adapted to generate a deinterleaved output in accordance with said decoded output signal input thereto;

a forward error correction decoder adapted to generate output receive data in accordance with said deinterleaved output signal input thereto; and

a controller adapted to manage and control said input means, I matched filter, Q matched filter, said processor, said decoder, said deinterleaver and said forward error correction decoder.

12. The apparatus according to claim 11, wherein said step of detecting the presence of signal activity comprises the steps of:

performing initial automatic gain control (AGC) on said signal;

performing signal decimation; and

performing signal detection and frequency acquisition.

13. The apparatus according to claim 11, wherein said step of acquiring said signal comprises the steps of:

inputting said signal to a first matched filter;

performing a first automatic gain control (AGC) acquisition;

performing timing acquisition;

inputting said signal to a second matched filter;

performing a second automatic gain control (AGC) acquisition;

performing fine frequency estimation; and

performing phase acquisition.

14. The apparatus according to claim 11, wherein said step of acquiring said signal comprises the step of performing coarse phase acquisition on said signal, wherein said step of performing coarse phase acquisition comprises the steps of:

rotating vectors  $z_n$  representing said signal into a single quadrant by an angle  $\Theta_k$ ;  
wiping off said  $z_n(\Theta_k)$  modulation;  
summing the wiped off vectors  $z_n(\Theta_k)$ ;  
determining the energy contained within a plurality of hypotheses; and  
5 selecting a single hypothesis from said plurality of hypotheses having the maximum  
energy.

15. The apparatus according to claim 11, wherein said step of pre-tracking comprises the  
steps of:

10 inputting said signal to a matched filter;  
performing automatic gain control (AGC) tracking;  
performing timing tracking;  
performing phase tracking;  
generating I and Q soft decisions; and  
determining whether signal lock has been achieved.

15 16. The apparatus according to claim 11, wherein said step of pre-tracking comprises the  
steps of performing timing acquisition on K groups, each made up of N DFT estimates, each  
estimate calculated from blocks of 16 symbols, said step of performing timing acquisition  
comprising the steps of:

20 calculating a timing estimate  $t_i$  based on a DFT for 16 contiguous symbols,  $i = 1, \dots, N$ ,  
thereby obtaining N DFT estimates each based on a block of symbols;  
generating a histogram of said N DFT estimates  $t_i$ ;  
classifying a timing range said group the N estimates are in based on said histogram;  
unwrapping said N DFT estimates and calculating their average  $T_i$ ; and  
unwrapping K average estimates  $T_i$  and performing a least square fit of said K  
25 averages so as to generate a final estimate.